REMARKS

The disclosure is objected to because of the following informalities: The word "accessis" in the fourth line of paragraph 0004 of page 1 is not a word. The same paragraph also utilizes double quotes where only an apostrophe is necessary. In paragraph 0005, the "of" is missing in line 11 in between "context" and "an EFM Waveform", where the "Waveform" does not need to be capitalized. In paragraph 0006 of page 3, the word "Laser" should not be capitalized. Appropriate correction is required.

Applicant has amended the specification to correct all the missing space errors caused by the electronic submission of the patent application. Also, all the specific errors indicated by the Examiner have been corrected in addition to numerous errors not specifically mentioned. The corrections involve adding missing spaces, capitalization, and punctuation, and also a few grammatical issues have been fixed as shown above in the "amendments to the specification" section. No new matter is added.

Claim 3 is rejected under 35 USC 112, second paragraph, as being indefinite because "second delay signal for delaying the second delay signal" portion of the claim is confusing. The claim has been interpreted as "to receive the second delay signal in order to delay the second delay signal according to the first clock signal and to receive the rough delay parameter in order to generate the first delay signal" by the examiner.

As explained below, applicant has amended claim 1 to include all the limitations of original claim 3 (and intervening claim 2). When merging claim 3 in to claim 1, applicant also corrected the wording of original claim 3 to make it less confusing. The same interpretation was used as was understood by the Examiner in the above-stated 112 rejection to claim 3. No new matter is entered.

Claims 1-7 and 9-18 are rejected under 35 USC 103a as being unpatentable over Kaku et al., US Patent 6,414,932, in view of Kato et al., US Patent 6,775,217.

Applicant has amended claim 1 to include all the limitations of claim 3 including

intervening claim 2. Claim 3 is correspondingly cancelled and claims 4-10 and 14-18 are amended to be dependent on claim 1. No new matter is entered. Applicant points out that the amendments to the claims involve only merging existing claims present in the original application as filed and therefore does not anticipate that the amendments to the claims will necessitate a new search by the Examiner. Applicant asserts that original claim 3 (currently amended claim 1) should not be found as being unpatentable over Kaku et al. in view of Kato et al. because neither Kaku no Kato teach all the limitations as claimed.

Additionally, the adjustment data storage unit is different between the present invention and the cited references. In the present invention, element 14 is for "selecting and outputting a corresponding set of write strategy parameters from plurality of the sets of write strategy parameters". However, as taught by Kaku et al. in column 5 lines 40-42, element 104 is able to generate a timing signal ... for selecting the Pa-Pd registers 106-109 (recording power). Therefore, the output of the adjustment data storage unit is the write strategy parameter in the present invention but the timing signal for selecting recording power as taught by Kaku et al. Besides, as taught by Kaku et al., the timing signal from element 104 is generated not on the basis of adjustment data mentioned in present invention, but by delaying the NRZ signal via element 114.

Furthermore, concerning the fine delay chain: in the present invention as shown in Fig.3, "the fine delay chain having a plurality of serially connected delay cells, each delay cell delaying the first delay signal by a predetermined period". However, as taught by Kato et al. in column 5 lines 1-3 and Fig.3, 324 is clocked from 320. Therefore, the implementation of the fine delay chain is different because no clock is needed in the present invention.

Concerning the second clock signal: in the present invention, the second clock signal is generated from the clock generator. However, in the circuit of Kaku et al. as shown in Fig.2 and described in column 5 lines 9-18, SCLK is a clock signal for the serial interface control unit 100, and the output of 100 are the setting values written into the corresponding registers. Therefore, the output of 100 does not include the clock

information according to the specification of Kaku et al.

Applicant notes that in the rejection to original claim 3, the Examiner (see Office Action dated 04/19/2006) did not provide any specific references to the cited prior art for the limitation: "for generating a rough delay parameter and the fine delay parameter according to the selected set of write strategy parameters", as is claimed in the present invention regarding the delay adjustment state machine. The Examiner stated in the first part of the rejection to claim 3 that the delay adjustment state machine is "part of element 114" of Kaku et al. However, when trying to combine the teachings of Kato et al. with Kaku et al., the Examiner switched the interpretation of the delay adjustment state machine to "duties performed by the 'write strategy delay table' of element 350". Applicant asserts that the inconsistent interpretation of exactly what element is being interpreted by the Examiner as being the delay adjustment state machine is evidence that there is no such element taught by Kaku et al. and Kato et al. Additionally, there is no mention of a rough delay parameter or a fine delay parameter taught by Kaku et al. or Kato et al. In particular, the output of 350 of Kato et al. are sent to rough delay unit 322 or fine delay unit 324 directly. However, in present invention, the output of adjustment data storage unit 14 is sent to delay adjustment state machine 20 first for generating rough delay parameter and fine delay parameter.

Furthermore, concerning the limitation "a rough delay counter or a rough delay shift register for receiving the first clock signal from the clock generator, and the second delay signal and the rough delay parameter from the delay adjustment state machine, wherein the rough delay counter or a rough delay shift register delay the second delay signal according to the first clock signal and the rough delay parameter to generate the first delay signal" included in currently amended claim 1, applicant points out that, except the first clock and N1, the input signals of the rough delay element 322 of Kato et al. are un-delayed EFM write pulses, not delayed signal. Therefore, element 322 of Kato et al. does not imply the rough delay counter 22 in our invention.

For at least these reasons, applicant asserts that currently amended claim 1 should not be found unpatentable by Kaku et al. in view of Kato et al. As claims 4–18 are dependent on

claim 1, if claim 1 is found to be allowable, so too should claims 4-18. Reconsideration of claims 1, 4-18 is respectfully requested. Further remarks concerning the patentability of specific dependent claims is providing below.

Concerning the patentability of claim 4, applicant asserts that Kaku et al. do not teach the limitation, "a frequency divider for dividing a frequency of the inputted first clock signal to generate the second clock signal". The Examiner stated that said limitation is taught by Kaku et al. in column 2, lines 18-32 and column 6, lines 44-49; however, inspection of these sections shows that there is no mention of a frequency divider or that the frequency of the inputted first clock signal is divided to thereby generate the second clock signal. For at least this reason, applicant asserts that claim 4 should not be found unpatentable in view of the teachings of Kaku et al. and Kato et al. Reconsideration of claim 4 is respectfully requested.

Concerning the patentability of claim 5, applicant asserts that Kaku et al. do not teach the limitation, "a period of the second clock signal is equal to a base period of the RLL modulation waveform." The Examiner stated that said limitation is shown in Figure 3(ii) as compared to figure 3(iv) concerning the clock signal (CLK SIGNAL). However, applicant points out that the Examiner previously defined the second clock signal to be SCLK (see rejection of claim 3). That is, Figure 3(ii) and (iv) of Kaku et al. are not showing having anything to do with the second clock signal SCLK. In particular, see Kaku et al. col 6, lines 41-42 stating, "Fig.3(iv) depicts a clock signal chCLK supplied from the modulation circuit 7". In other words, using the same interpretations made by the Examiner in the rejection of claim 1, Fig.3(iv) is the first clock signal of the present invention not the second clock signal. For at least this reason, applicant asserts that claim 5 should not be found unpatentable in view of the teachings of Kaku et al. and Kato et al. Reconsideration of claim 5 is respectfully requested.

Concerning the patentability of claims 6 and 9, applicant asserts that Kato et al. do not teach the limitations: "a period of the second clock signal is equal to a multiple of a period of the first clock signal" and "a resolution of the rough delay counter delaying the second delay signal is equal to a period of the first clock signal " because, according to the interpretations

made by the Examiner in the rejection of claim 3, the second clock signal is the signal SCLK of Kaku et al. Applicant points out that this is a serial clock to control serial interface unit 100, and Kato et al. does not mention such a device or anything about the clock signal for such a device. For at least this reason, applicant asserts that claims 6 and 9 should not be found unpatentable in view of the teachings of Kaku et al. and Kato et al. Reconsideration of claims 6 and 9 is respectfully requested.

Claim 8 is rejected under 35 USC 103a as being unpatentable over Kaku et al. in view of Kato et al., as applied to claim 3 above, and further in view of Chung et al., US Patent 4,873,680.

Applicant points out that currently amended claim 8 is dependent on claim 1, which is believed to be allowable for at least the above-stated reasons. Therefore, claim 8 should also be allowable for at least the same reasons. Reconsideration of claim 8 is respectfully requested.

Sincerely yours,

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